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Low Power High Speed Power Gating Structure with Intermediate Sleep Mode for Single V_t CMOS Circuit

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ABSTRACT
To reduce the wake up time and leakage power, we have realized the power gating structure with intermediate sleep mode. In this technique, we operate the sleep transistor at gate voltage ($0 < Vg < V_{th}$) during sleep mode. Due to which the virtual ground node potential (Vgnd) of the sleep transistor decreases. This reduction in Vgnd reduces the wake up time. But at the same time, the reduction in Vgnd increases the leakage current by some amount. So, the optimum point is obtained by varying Vg from 0 to V_{th}, which provides the minimum wake up time and leakage current in the circuit. In addition to the minimization of wake up time, operating the circuit at this optimum point limit the maximum value of short circuit current. To establish the usefulness of proposed approach, the power gating structure with intermediate sleep mode has been compared with conventional structure. Simulation result shows that power gating structure with intermediate sleep mode can provide 20% reduction in wake up time and 45% reduction in short circuit current as compared to conventional power gating structure.

Keywords - leakage current, power gating, power mode transition,short circuit current, wake up time.

I. INTRODUCTION

Power consumption is one of the top concern of Very Large Scale integration (VLSI) circuit design, for which Complementary Metal Oxide Semiconductor (CMOS) is the primary technology. Power consumption of CMOS consists of dynamic and static components. As the technology is shrinking static component is becoming dominating component as compared to dynamic component. Static power dissipation is mainlycontributed by sub threshold current conduction, Band to Band tunneling current, punch through and Gate oxidetunneling. The sub threshold current is predominant of the entire leakage current source and becomes extremely challenging for the researchers and future silicon technologies.

There are several different techniques that can be used to tackle the leakage from various angles [1]-[6].Power gating is one well known way of reducing leakage, and it continues to be applied to very deep sub micrometer CMOS technologies. There has been a lot of work [7]-[9] on power gating structure technique, which uses the MOSFET switch to gate or cut off , a circuit from its power rails during standby mode. However, without a clear understanding of the technique, the negative effect of power gating and the range of device options may overwhelm the potential benefits. The power gating switch is typically positioned between the circuit and the power supply rail or between the circuit and ground rail.

During active operation, the power gating switch remains on, supplying the current that the circuit uses to operate.

During standby mode, turning off the power gating structure reduces the current dissipated through circuit. Since the switch gates the power when the circuit is in standby mode, it is commonly called a sleep transistor [10]-[11].

By turning off the sleep transistor during sleep period, all the internal capacitive nodes of the logic blocks and the virtual ground rail charge-up to a steady state value close to $V_{DD,}$ strongly suppressing leakage current. However, when the virtual ground rail is restored to its nominal value, there is a potentially significant "wake up" overhead associated with discharging the virtual ground rail capacitance back to ground [12]-[13]. Because of sudden discharge of virtual ground rail capacitance a significant amount of short circuit current flow in the circuit. Additionally, waking up a logic block affects other nearby logic through ground bounce due to large associated instantaneous current spike that occur while discharging the virtual ground rail[14]-[16]. In this paper, basically these problems have been explored, and a robust power gating structure with effective power mode transition strategy is presented.

II. POWER GATING STRUCTURE

In this technique, a sleep transistor isadded between the actual ground rail and circuit ground (called virtual ground) [7]. Sleep transistors

disconnect logic cells from the power supply and/or ground to reduce theleakage in sleep mode. More precisely, this can be done by using one pMOS transistor andone nMOS transistor in series with the transistors of each logic block to create a virtualground and a virtual power supply as depicted in the left-hand side of Fig. 1. In practice,only one transistor is necessary. Because of the lower on-resistance, nMOS transistors areusually used. In the ACTIVE state, the sleep transistor is on. Therefore, the circuitfunctions as usual. In the STANDBY state, the transistor is turned off, which disconnectsthe gate from the ground.

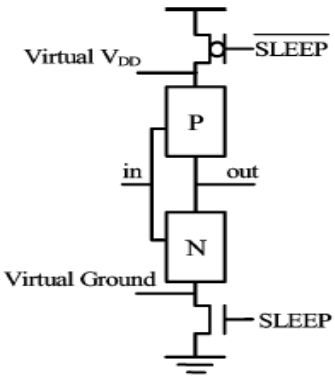

Fig 1. Power gating structure

Active mode: When our logic circuit is in use, or some switching activity is happening inthe circuit, then this mode of operation is known as active mode. During the active mode, SLEEP =1 and sleep transistor is on.

Standby mode: When our logic circuit is not in use or no switching activity is happening,then the logic circuit is said to be in Standby mode or sleep mode.In this mode sleep= 0 and both the sleep transistor will be turned off.

III. KEY OBSERVATIONS

It is a well-known fact that there is no need to have both nMOS and pMOS sleep transistors to encapsulate a logic cell. In particular, nMOS sleep transistors can be used to separate the (actual) ground from the virtual ground of the logic cell.

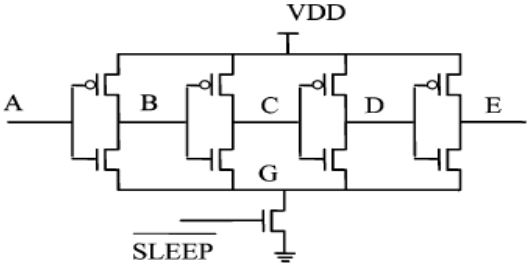

Fig 2. Chain of four inverter with an nMOS sleep transistor

Consider the inverter chain shown in Fig. 2 which is connected to the groundthrough an nMOS sleep transistor. If the input of the circuit is low, then, in the active mode (i.e. SLEEP=l), V_A= Vc= V_E= V_G = 0, and Vs= Vo =V00. When entering the sleepmode, the voltages of B and D do not change, but the voltages of C, E and Ggradually increase and will be equal to nearly V_{DD}, if the sleep period is long enough (notethe driver of signal A is not controlled by the SLEEP signal). This happens because theleakage through the pMOS transistors will charge up all the floating capacitances. Becauseof the charging of virtual ground rail capacitance the following effects will occur in thepower gating structure.

A. Wake Up Time

Wake up time is the time required to turn on the circuit upon receiving the wake upsignal [12]. As it is explained that because of leakage current through pMOS transistor thevirtual ground node (G) capacitance will charge up to a steady state value near V_{DD} .During mode transition, while turning on the sleep transistor, virtual ground rail
capacitance discharges to restore its nominal value. So, there is a potentiallysignificant "wake-up" time associated with discharging the virtual ground rail capacitanceback to ground. Higher the value of Vgnd higher the wake up time.

B. Short circuit current

As it is explained the voltages of C, E and G gradually increase and will be equal to nearly V_{DD}. During mode transition voltage of G quickly reaches its final value, the voltages of C and E are still between zero and V_{DD}. This results in a significant amount of short circuit current in the logic cells driven by nodes C and E since these nodes turn on both transistors of the inverters present in their fanout. The. current flowing through the sleep transistor is the result of not only discharging the accumulated charge in some intermediate nodes (i.e. , C, E and G in the inverter chain), but also the short circuit current flowing through some logic cells ofthe circuit (e. g., the third inverter in the chain which is driven by signal C) flows The short circuit current in the circuit depends upon the amount of charge it has to discharge during mode transition, which in turn depends upon the virtual ground node potential(Vgnd). Higher Vgnd results in higher short circuit current.

C. Ground Bounce

The amount of instantaneous current that can flow through the sleep transistor during mode transition is much larger than the active mode current. The current surge creates inductively

induced voltage fluctuations in the power distribution network [16].

IV. POWER GATING STRUCTURE WITH INTERMEDIATE SLEEP MODE

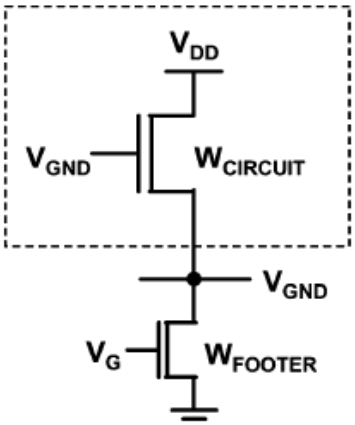

Fig 3. Simplified circuit for V_{gnd} model

Let us assume that the during sleep mode sleep transistor operates in the weak inversionregion and the leakage of the logic circuit can be approximated by the leakage of a singletransistor of effective width Wcircuit Under the assumption that the sleep transistor isbiased in the weak inversion region, the steady state potential Vgnd can be obtained by matching the leakage current of the logic circuit with the leakage of the sleep transistor.

$$I_{leakage}(\text{circuit}) = I_{leakage}(\text{sleep}) \quad (1)$$

$$\text{Vgnd} = \frac{-\text{Vg} + \text{Sslog}\left(\frac{\text{Wcircuit}}{\text{Wsleep}}\right) + \eta V_{DD}}{2\eta} \quad (2)$$

Here, η is the DIBL coefficient, Ss is the subthresholdslope, V DD is the supply voltageVg is the gate voltage of sleep transistor, Io is constant, Vgnd is the virtual ground voltage,$Ws_{leep}$is the sleep transistor width, Wcircuit is the width of the logic circuit.

Theequation (2) shows that the steady state Vgnd is linearly dependent on sleep transistorgate voltage Vg with a negative slope. If the footer gate voltage is increased, it results in a decrease in the virtual ground potential and vice versa. Hence, Vgnd potential in the sleepmode can be effectively controlled by the gate voltage of the sleep transistor. So, Vgnd can be effectively controlled by Vg of sleep transistor.

So far now, we operate the circuit only in two modes sleep mode (Vg=0V) and activemode (Vg=V_{DD}). But by exploiting the equation (2) we can operate the circuit withintermediate sleep modes with voltage range (0 < Vg < Vth). And each mode represent adifferent tradeoff between wake up and leakage saving. And there exist an optimum pointwhere we get minimum wake up time and minimum leakage. Impact of power gating structure with intermediate sleep mode on various parameter are as follow.

A.Wake up time

$$T_{wakeup} = \frac{Cc.V_{gnd}}{I_{on}} \quad (3)$$

Here, Ion is the on current of sleep transistor during turn on.

From equation (3) we can see that wake up timeincreases with Vgnd and vice versa. So, onoperating sleep transistor at optimum point with gate voltage (0 < Vg < Vth) Vgnd decreases by equation (2). And hence wake up time also get reduced.

B. Short circuit current

If the circuit is operated at optimum point then Vgnd will be reduced by equation (2). So, the total amount of charge which needs to be dischargeddecreases, which in turn decreases the amount of short circuit current that flows in thecircuit.

C. Ground Bounce

The ground bounce depends upon the short circuit current. If the short circuit current gets reduced then the groundbounce can also be reduced. So, by operating the circuit at optimum point short circuit current getsreduced,which in turn reduces the ground bounce in the nearby circuit.

D. Leakage Current

Power gating structure controls the leakage current by raising the virtual ground node potential. Thereby decreasing the effective voltage across the logic during sleep mode andleads to reduction in leakage current. So, larger the value of Vgnd larger is the leakagesavings. But by operating the circuit at optimum point (0 < Vg < Vth) virtual ground nodepotential decreases which increases the leakage current by some amount.

So, the power gating structure with intermediate sleep mode shows a significantimprovement over the conventional power gating structure in terms of wake up time, shortcircuit current and ground bounce. However leakage current increases by some amount inthe former case, but thatcan ignore because of all the advantages what we get in thiscase.

V. SIMULATION RESULTS AND ANALYSIS

To substantiate the importance of this topology, the chain of four inverters (fig. 2) withsleep transistor in 0 .2 5 um and 0.l 8um technology has been simulated. The supply voltage is 2.5 V and l .8V respectively. The following observations has been made from the simulation results.

A .Virtual Ground Potential

Virtual ground potential (Vgnd) is the key parameter to control the wake up latency and leakage current in power gating structure. Fig 4 and 5 shows the effect of sleep transistor gate bias (Vg) on Vgnd for 0.25umand 0.18um technology. From the figure we can observe that on increasing Vg from0 to Vth, the Vgnd has been decreasing approximately linearly. Noteworthy point is that for 0.25 um technology Vgnd is decreasing only for the voltage range (0 < Vg <0.35 V) subsequently it becomes constant. For 0.18um technology range is (0 <
Vg < 0.3V).

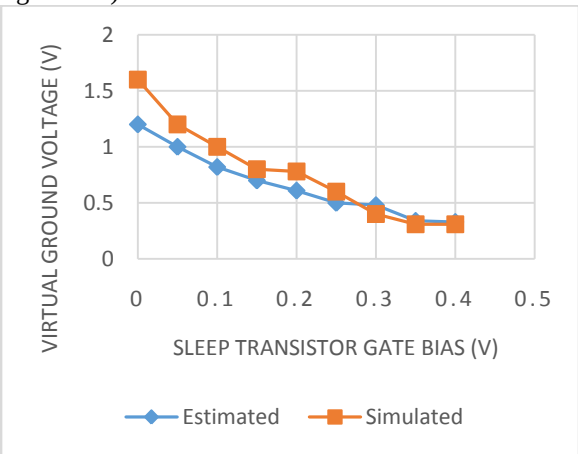

Fig. 4 Effect of Sleep transistor gate bias voltage on virtual ground potential (0.25 um)

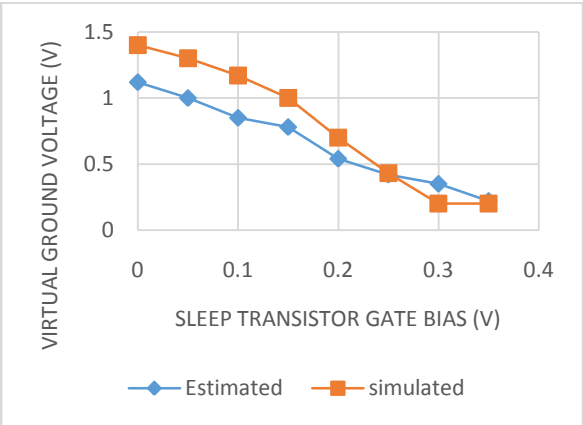

Fig. 5 Effect of Sleep transistor gate bias voltage on virtual ground potential (0.18 um)

B. Wake up time

It is the time required to turn on the circuit upon receiving thewake up signal. Its dependence on the virtual ground potential (Vgnd) can be given by equation(3), which clearly depicts that wake up time increases with Vgnd andVgnd as shown in figure 4 and 5 decreases with V g. Hence wake up timedecreases with V g.

C. Leakage versus wake up time trade off

Leakage current is control by raising the virtual ground nodePotential Figure 6 and figure 7 shows leakagecurrent versus wake up time tradeoff. As wake up time decreases with Vg and leakage current increases with Vg, So there exist a optimum point where we get minimum wake up time and minimum leakage current. For 0.25um technology optimum point is V g=0.1 7V and for 0.18um technology optimum point is Vg=0. 19V. However, by operating the circuit at this point leakage current increases bysmall amount, but at the same time reduction in wakeup time is also achieved whichis the main area of focus. Percentage reduction in wake up time by operating thecircuit at optimum point as compared to base case i.e. Vg= 0V is 16% for 0.25umtechnology and 20% for 0.18um technology.

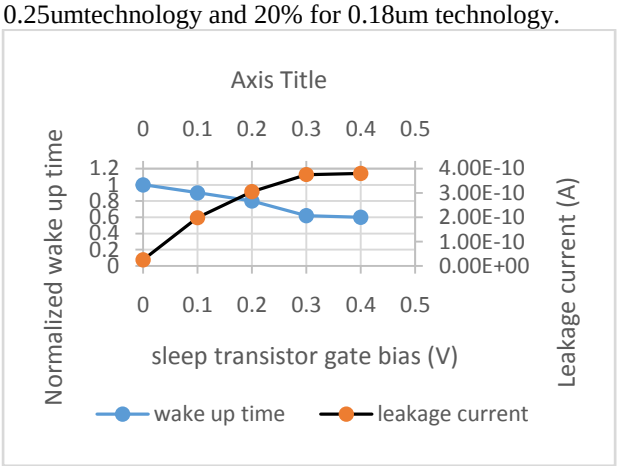

Fig. 6 Leakage current Vs wake up time tradeoff (0.25um)

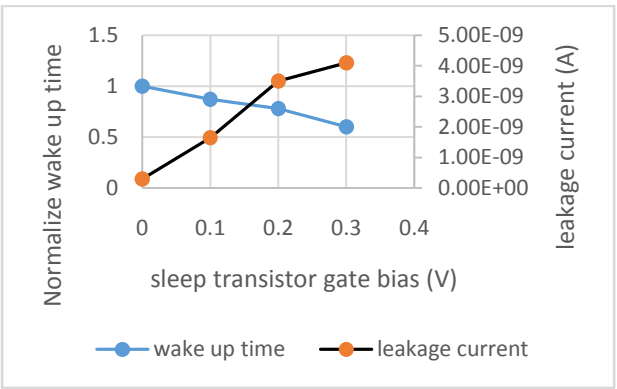

Fig. 7 Leakage current Vs wake up time tradeoff (0.25um)

D. Short circuit current

It is the total current which flows to the ground during modetransition [14]. It also depends on the virtual ground potential. Higher the value ofVgnd larger the short circuit current in the circuit. Because it has to discharge morecharge to the ground during mode transition. On operating the circuit at V g= 0 .17i.e. at optimum point, the Vgnd is less as compared to base case Vg= OV. So, areduction in short circuit current is also obtained by operating the circuit atoptimum point

E. Ground Bounce

By turning off the sleep transistor during the sleep period, all theinternal capacitive nodes of the logic blocks and the virtual ground rail charge-up to a steady-state value close to V_{DD}. And during mode transition because of the sudden discharge of virtual ground rail capacitance a significant amount of shortcircuit current flow in the circuit. This short circuit current creates current surgeselsewhere. Because of the self-inductance of the off-chip bonding wires and theparasitic inductance inherent to the on-chip power rails, these surges result involtage fluctuations in the power rails. If the magnitude of the voltage surge ordrop is greater than the noise margin of a circuit, that circuit may erroneously latchto the wrong value or switch at the wrong time. This is known as ground bounce. Ground bounce depends on the short circuit current flowing in the circuitduring mode transition. If short circuit current is less than the ground bounce canbe reduce. From the results we can see that by operating circuit atoptimum point,the short circuit current has been reduce, so the proposed techniquereduces the problem of ground bounce also .

Table.1 and 2 represent the reduction in wake up time and short circuit current at optimum point as compared to base case V g = 0V in the chain of four inverter.

Table 1. Summary of results for 0.25 um technology

	Base case(Vg=0V)	**With intermediate sleep mode (Vg=0.17V)**	**% Reduction**
Normalized wake up time	1	0.84	16%
Short circuit current	142uA	100uA	30%

Table 2. Summary of results for 0.18um technology

	Base case(Vg=0V)	**With intermediate sleep mode (Vg=0.19V)**	**% Reduction**
Normalized wake up time	1	0.80	20%
Short circuit current	190uA	100uA	45%

VI. CONCLUSION AND FUTURE SCOPE

To reduce the wake up time and leakage power, we have realized the power gatingstructure with intermediate sleep mode. In this technique, we operate the sleep transistor atgate voltage ($0 < V g <$ Vth) during sleep mode. Due to which the virtual ground nodepotential (Vgnd) of the sleep transistor decreases. This reduction in Vgnd reduces the wakeup time. But at the same time, the reduction in Vgnd increases the leakage current by someamount. So, the optimum point is obtained by varying Vg from 0 to Vth, which providesminimum wake up time and leakage current in the circuit.

In addition to the minimizationof wake up time, operating the circuit at this optimum point limits the maximum value ofthe short circuit current. Reduction of short circuit current also reduces the voltage fluctuation in power rail. To establish the usefulness of proposed approach the powergating structure with intermediate sleep mode has been compared with the conventionalstructure. In conventional power gating structure, we operate the sleep transistor at Vg=0Vduring sleep mode. Simulation results for the proposed approach shows that by operatingthe circuit at Vg=0.17V, 16% reduction in wake up time and 30% reduction in total shortcircuit current is obtained for 0.25um technology as compared to base case Vg = 0V.Whereas 20% and 45% respectively reduction is obtained for 0.18um technology at Vg =0.19V as compared to base case. The proposed approach can significantly improve theperformance of single Vt CMOS circuits in terms of wake up time and leakage power.

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